The Development of the New Low Resistive Material Bus-Line Process with Super High Aperture Ratio for High Resolution TFT-LCDs

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Abstract

The TFT-alley process for high resolution and large screen size TFT-LCD such as 20UXGA (1600x1200) is developed without the need for extra processing steps. A demonstrated novel process uses Pure-Al metal as gate and source electrode with low dielectric interlayer, which can result in achieving high performance a-Si TFT with high yield. 18.1SXGA(1280x1024) panel was already introduced in the mass production and achieved high cost performance with high aperture ratio.

Introduction

The demand of the large screen with high-resolution panel would be increased and these panels could be utilized for note, desktop and digital TV applications. High resolution and large screen size TFT-LCD panels require a longer gate line, which affects the RC time delay of the gate signal. As a result, low resistivity material should be proposed. High conductivity gate metal such as Cu is highly desirable, but Cu is difficult to implement due to poor adhesion to glass, reaction with Si and difficulties in contacting it to other metals. High conductivity material such as Al or Al-alloy is another candidate. However, pure-Al also have several serious issues. For example, it is well known that it easily produces defects such as hillocks and chemical corrosions. These defects can degrade the product's quality, as well as production yield. To prevent these serious issues, several approaches are proposed. For instance, full capping Al process is proposed. However, a full capping process requires two lithography steps, two deposition steps and two etching steps. And also Cr capping process such as Cr/Al, Cr/Al-Nd is proposed. These processes have an advantage to be able to etch Cr/Al(Al-Nd) at the same time using wet etching. However, the wet etching of Cr has environmental issue so that it requires special treatment for Cr waste fluid. On the other hand, a single Al-gate process is also proposed using Al-Cu, Al-Si and Al-Si-Cu. It is also reported Al-Ta and Al-Ti are being used for mass production. However, both alloys don't have low resistance enough to be used for high-resolution panels.

For this work, novel Al gate and source process is demonstrated to avoid Al process issue. The typical problem associated with the use of Al (hillocks, Al corrosion, Oxidation) is investigated. The gate Al is etched by using dry etching without the need for extra processing steps. The acrylic rein process is combined for preventing Al corrosion. Furthermore, the novel Al process uses only six-mask, which means that it achieved high cost performance without extra steps.

1. Process flow

The process was demonstrated by fabricating 20UXGA displays (1600x1200) on 560x650cm corning 1737 glass. The complete process flow is shown in **Fig. 1**.

Pure-Al is selected both gate and source-drain bus-line. TiN/Al/Ti gate metal is deposited on the corning 1737 glass by using sputtering with multi-chamber system. The advantage of applying Al/Ti layer is that a (001) Ti texture enhances Al (111) texturing. In addition, due to the smooth surface of the glass, the surface roughness of Al is decreased when it is deposited on the highly oriented (001) Ti underlayer. The TiN-capping layer on Al/Ti is necessary to prevent Al hillocks and better adhesion to Gate insulator (SiNx). After deposition of the gate

electrode, photo-resist is coated and patterned by using conventional photolithography tool. (First photo mask). TiN/Al/Ti gate with photo resist is etched by reactive ion etching (RIE) continuously. The RIE tool is suitable for TiN/Al/Ti continuos etching because there is no significant difference in the etch rate between Al and Ti. Therefore, the tapered profile is controlled. Al corrosion was observed after dry etching using Cl_2/BCl_3 gases at the experimental stage. It is well known that the remaining Cl gas on the Al film reacts with moisture immediately after dry etching and Al (OH_3) are then created. To eliminate the remaining Cl, a CF_4/O_2 treatment is applied to the post process. **Fig. 2** shows Al corrosion after resist striping.

The gate etching is optimized for decreasing Al corrosion using CF_4 gas flow. **Fig. 3** shows CF_4 flow ratio as a function of Al corrosion.

The Al corrosion is disappeared with the optimized etching process when CF_4 flow rate exceeds 100sccm.

After deposition of the gate insulator I-Si and n+ films, the TiN/Al/Ti gate surface and tapered profile are observed with microscopes. No hillocks are observed both surface and tapered profile even on the thinner Ti top layer. **Fig. 4** shows a gate profile with gate insulator.

N+/I-Si dual layer is patterned and etched using conventional method (2nd mask). After patterning of n+/I-Si, the gate insulator (SiNx) is patterned (3rd mask) and etched for making contact hole where is connected with Tabs in the peripheral area. Al/Ti dual layer is deposited continuously by conventional sputtering as a Source-Drain electrode. The lower layer (Ti) has two main important parts besides enhancing Al (111) texturing. One is that Ti layer is utilized as a Si blocking layer. The other important part is that Ti film is used contacting layer with pixel ITO film. The capping layer isn't necessary to surpress hillocks because of weak thermal stress (as high as 250 degree C) following alley process. After source-drain electrode is patterned (4th mask), Al film is etched by wet etching using conventional Al etchant. Then, Ti/n+ dual layer is etched by RIE. Source-drain electrode and TFT (thin film transistor) channel region, which is between source and drain electrode, are patterned simultaneously. In the case of experimental process, the etching of Al/Ti/n+ stacked layer and/or selective etching between Ti and n+ layer are possible. However, to achieve uniformed TFT characteristic even large substrate, Al film should be removed to reduce etched thickness. The left I-Si thickness in the channel region is highly important factor to have uniform TFT characteristics. Therefore, the combination of wet and dry etching method is high advantage for mass production. After patterning TFT and source-drain electrode, SiNx passivating layer is deposited by using PE-CVD. As a following process, a low dielectric interlayer (acrylic resin) is coated by conventional

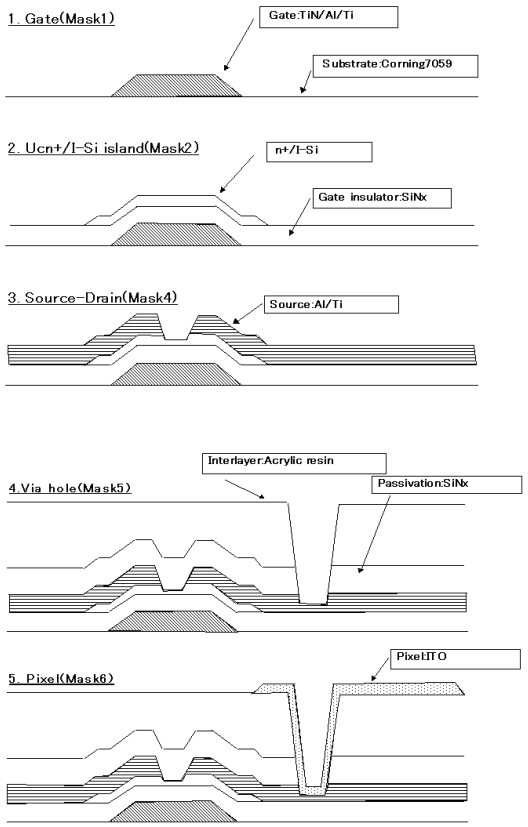

Fig. 1 Process flow
(Al-damage free structure for the reason of thick interlayer resin.)

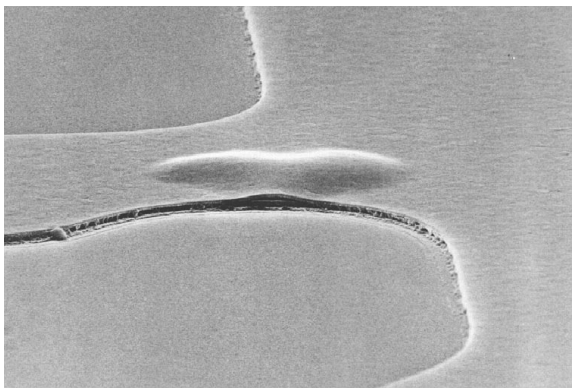

Fig. 2 Typical Al corrosion after stripping.

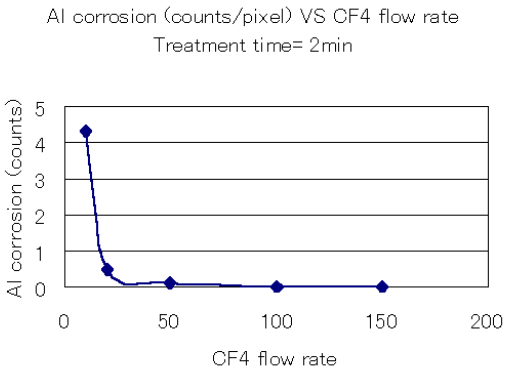

Fig. 3 Al corrosion VS CF4 flow ratio.

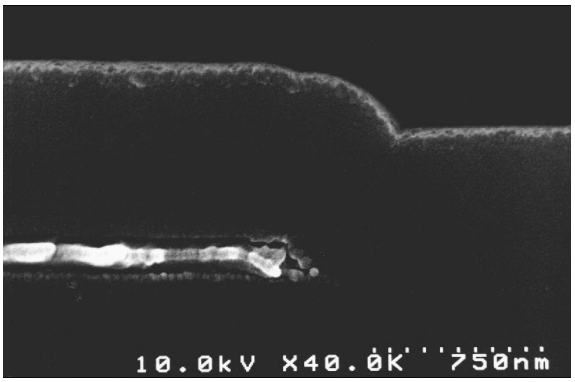

Fig. 4 Gate profile with Gate insulator.

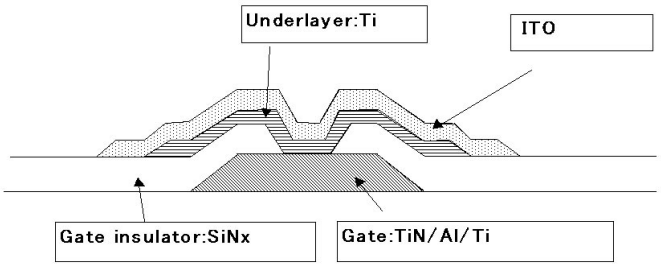

Fig. 5 Cross section view of Tab region.

lithography and patterned for making via hole (5th mask). Passivation film is etched by using plasma etching. Tapered etching is required to improve step coverage for pixel electrode. After etching of passivation film, bared Al layers at the drain electrode and Tabs region are removed to improve contact resistant. **Fig. 5** shows the cross sectional view of the Tab region consists with ITO/Ti/TiN/Al/Ti.

Therefore, ohmic-contact between pixel electrode and drain electrode is ensured. After removing Al film, ITO film is deposited by conventional sputtering as a pixel electrode. Then ITO film is patterned (6th mask). Pixel electrode is usually etched using strong acid such as HCl, HBr. Al Gate and Source-drain electrode is corroded when additional interlayer such as acrylic resin, poly-imido is UN-coated. Making pinhole free insulator consisting of gate insulator and TFT passivation is important point to utilize Al efficiently. Thicker interlayer characterizing low dielectric such as acrylic resin is suitable candidate to achieve pinhole free layer. **Fig. 6** shows TFT characteristics through Al gate Source process.

Therefore, the combination of Al gate and source bus line with low dielectric insulator result in processing defect free.

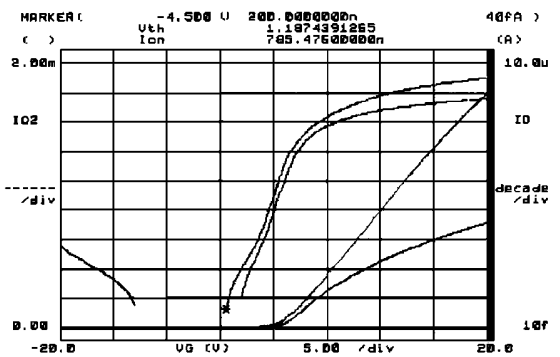

Fig. 6 TFT characteristics.

Conclusion

20"UXGA (1600x1200) panel is demonstrated with Al gate and source electrode using six mask process. The demonstrated TFT process, which characterized pinhole free consisting of gate insulator, TFT passivation and acrylic interlayer resin can be prevented Al corrosion perfectly. The Al hillocks are suppressed by the stress compensation effect of the capping TiN layer. To improve contact resistant between ITO and Al layer at both pixel and pad region, Al layer is removed. Therefore, Ti under-layer is necessary to solve contacting problem between ITO/Al interface. Higher aperture ratio (60%) is also achieved through this process. We propose that simple Al metallization technology with low dielectric interlayer is the most suitable process for large area TFT-LCDs with high yield. In addition, the developed novel process can be applied to large panel display with higher resolution. Our future plan is that to demonstrate large screens Digital TV with high aperture ratio. We hope that it replaces conventional cathode-ray tube until 2005 years.

References

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