Development of New Driving and Packaging Methods for LCD Driver LSIs

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Abstract

In the conventional AMLCD, input signals are directly fed into each cascaded driver LSI.
The authors developed new driving and packaging methods in which only the top driver LSI gets signals from the control LSI, which are then transmitted in cascade to the other driver LSIs (high-speed self-transfer).
The new methods enable the signal lines to be implemented on the LCD glass and this leads to a narrower frame and a thinner panel.

Introduction

Plural driver LSIs (gate driver and source driver) are used for large size AMLCDs with cascade connection according to the number of dot pixels in the module.
Usually only the operation starting signal of each LSI is transferred one after another, and all of the other display signals are inputted into all driver LSIs equally and individually.
Therefore, a PWB in source driver side needs to supply 18-bit data (for 64 gray scales) and clock signals to each source driver LSI. We must use plural layer board for PWB against EMI effect, because these signals are high frequency (65MHz for XGA).
The 2-port data input method is adopted to decrease data transfer speed for EMI effect reduction, but in this case, 36 data-bus is necessary to drive LSIs.
And in the case of PWB in gate driver side, usually power supplies must be connected to the gate driver LSIs individually through PWB.
The size of PWB in source driver side and gate driver side make significant limitation on module size reduction, and disturb a narrower frame and thinner module design.
To solve these problems, we have developed new types of driver LSIs with new high-speed self transfer technology, new TCP technology and new assembling methods.
Structures of the source driver and the gate driver are shown in **Photo 1** and **Photo 2**.

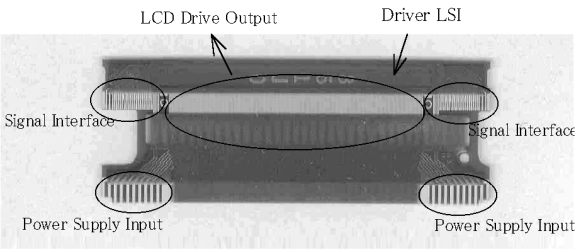


Photo 1 Structure of Source Driver.

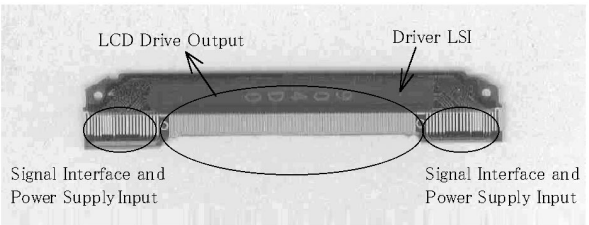


Photo 2 Structure of gate driver.

1. High-speed self transfer technology

We used eight 312-output source driver LSIs for the XGA panel. For receiving display data signals without error in the driver LSIs, tCK was used to satisfy the timing relation shown in **Fig.1**.
We adopted the following 3 technologies to satisfy these specifications.

(1) Dual edge data input

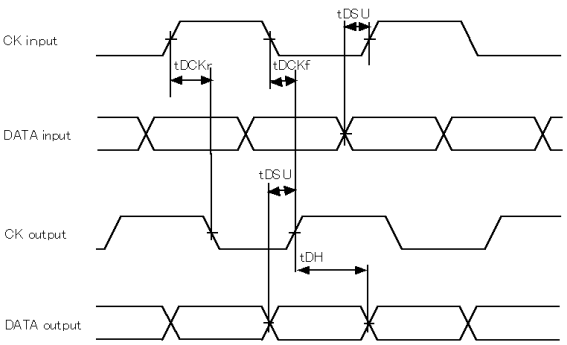
We adopted to receive data at both edges of the clock CK (rising edge and falling edge) to reduce frequency at the interface by half. If driver LSI's internal circuits are operated at this same timing, it is difficult to secure the clock duty ratio inside of the driver LSIs, so it is in danger of causing a reduction of the operation frequency. Then an operation that uses both edges of the clock is used for only the interface circuit, and we attempted to extend the operation frequency by converting data signals from serial to parallel in the input circuit, and from parallel to serial in the output circuit.

(2) Data transfer with polarity reversal

CK is used to receive data signals using both edges of the clock, and used to keep timing with display signals data. These signals secure the timing tDSU and tDH. (shown in **Fig.1**)

This technology prevents changing the duty ratio of signals when self-transmitting clock and data signals. If it repeats transmission without reversing the polarity, difference of the clock ratio becomes 7*|tDCKr-tDCKf| in the 8th chip. |tDCKr-tDCKf| is the difference of duty ratio. Therefore, it is difficult to operate the high-speed cascade transmission.

Therefore, we made the timing of the duty ratio less than |tDCKr-tDCKf| to correct the duty ratio with pair of driver LSIs by polarity reversal. The data signals are same.



tCK = (n−1) × | tDCKr − tDCKf | + tDSU(or tDH) + tCK(DUTY)
tCK : Clock period
n : Nmbers of LCD drivers
tDSU : Data set up time
tDH : Data hold time
tDCKr : CK delay time(rise edge)
tDCKf : CK delay time(fall edge)

Fig. 1 Timing chart of source driver.

(3) The self-coordinate circuit between signals in the chip

Driver LSIs need 19 signals (RGB x 6 and clock) that can display 64 gray scales.

In the case of conventional methods, these signals are input to every chip in the same timing as the control LSI.

Because of this it is not necessary to prescribe the difference in timing between the chips.

However, in the case of self-transfer methods, there is a dangerous possibility causing a difference in timing between the signals in every chip.

Therefore we adopted a circuit to coordinate the timing in every chip.

It is possible for us to compatible with an XGA panel through the adoption of these new technologies.

2. TCP assembly of source driver LSIs

The characteristic for the assembly of new source driver LSIs is developed of the assembly on the glass substrate. The new source driver LSI has input and output pins position different from conventional driver LSIs. (shown in **Fig.2**)

In the case of the conventional assembly, the output of driver LSIs are connected to the edge of the glass and to assembled chips outside of the glass.

In case of the new assembly, the source driver LSI is assembled on the glass, and connected to the output signal at the edge of the glass, and arranged data signals for outside of this because of all signals are translated by using pattern on the glass. And power supplies are given from PWB in source driver side. (shown in **Fig.3**)

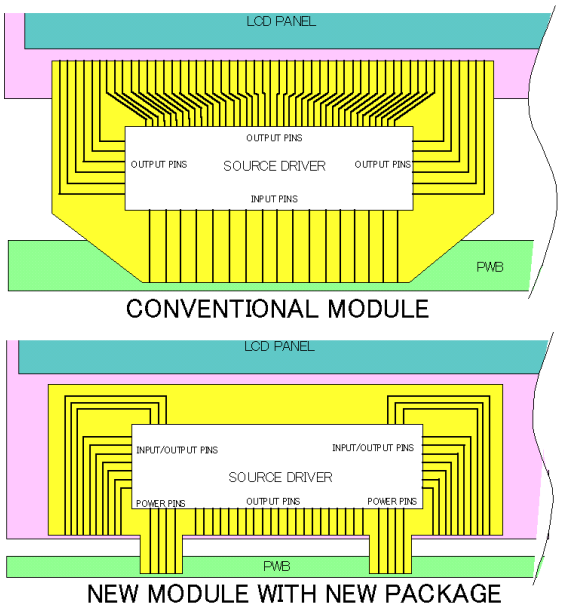


Fig. 2 Structure assembly for source driver.

To make the assembly method possible, we unified the terminal arrangement pitch on TCP and PAD pitch in the LSI to 50 micrometers—the smallest size in the industry. This made possible to miniaturize the TCP size.

3. TCP assembled for gate driver LSIs

The gate driver's frequency is very slow compared with the source driver's one, and its self-transfer signals are only clock and operation start signal. However, it needs plural power supplies to drive the active element for the LCD panel and the logic circuit. In the case of the conventional driver LSI, the power is supplied from PWB in gate driver side. But if the PWB were to be reduced, it could contribute to the miniaturization of the module.

To realize module miniaturization, we adopted a unique TCP pattern by inputting plural power supplies not only to the first driver LSI, but also to the next driver. (shown in **Fig.4**)

The connected method of this gate driver TCP is the same as that of the source driver.

4. Assembly of the LCD driver LSIs on the panel

A figure of the assembly for the source driver LSIs and the gate driver LSIs on the module is shown in **Fig.5**

Conventional modules have PWBs to input signals and power supplies. Input signals from control LSI are input to every driver

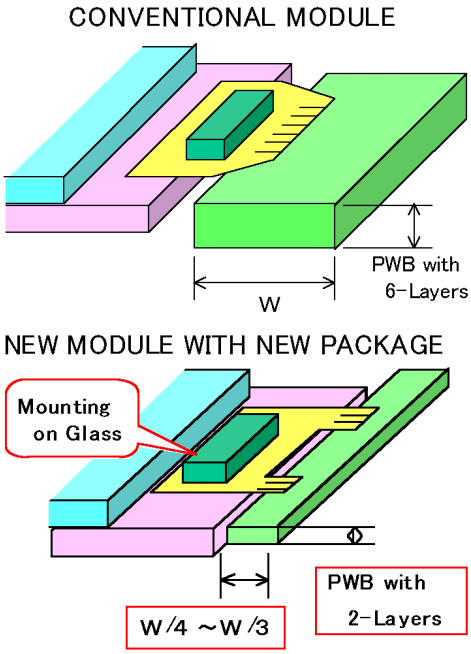


Fig. 3 Assembly source driver LSIs for panel.

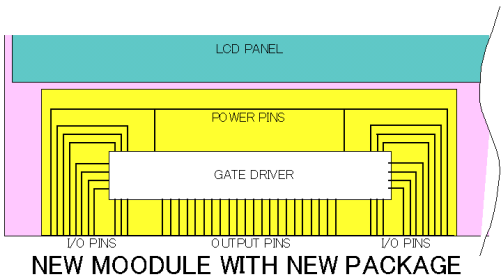


Fig. 3 Assembly source driver LSIs for panel.

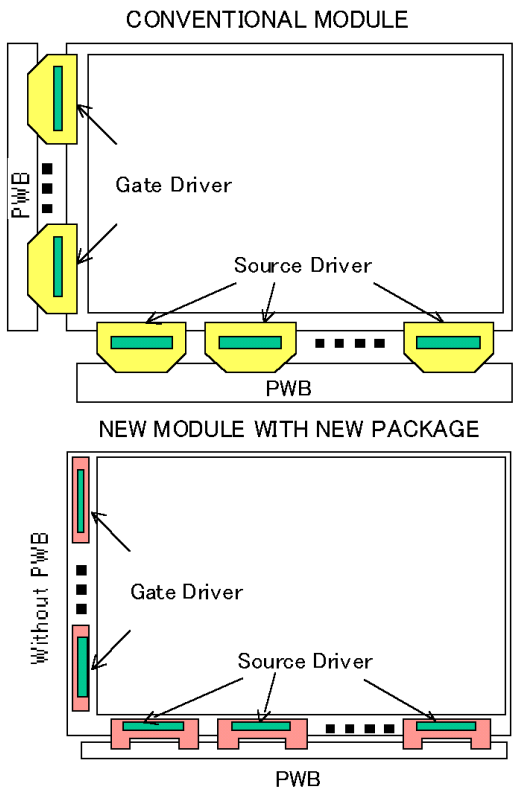


Fig. 5 Assemble driver LSIs for module.

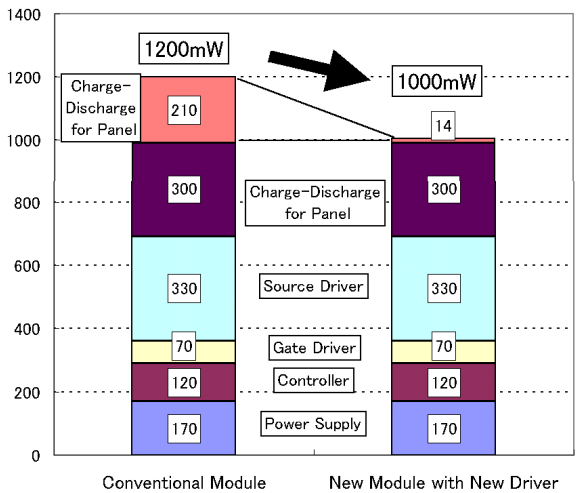


Fig. 6 Charge-discharge current for board.

LSI through the PWB.
The PWB in source driver side is made with multiple structure, but the size of PWB may be big depending on the number of input signals.
On the other hand, in case of a newly assembled module, input signals from the control LSI are input to only the first driver LSI near the control LSI without using a PWB. The second driver LSI's input signals are transmitted through the first driver LSI and so on after third driver.
The PWB in source driver side is designed only with power supply lines, so it is possible to reduce PWB to about W/4~W/3 as shown in **Fig.3**. Also, the charge and discharge current of PWB patterns is reduced, so it is possible to achieve low power consumption for total of module as well as lower EMI. (shown in **Fig.6**)
In the case of the gate driver LSI, same as the source driver LSI, almost all of the signal lines and power supply lines connect the inside of TCP, so it is possible to omit PWB.

Conclusion

The main specifications of the LCD driver LSIs developed at this time are shown in **Table 1** and **Table 2**. We are producing an LCD module which uses these LSIs.
We realized this new LCD driver through the fusion of high-speed self-transfer technology and TCP assembly technology. Using this new driver technology, this new module has higher durability to vibration and higher reliability than conventional TCP module, because the LSI chip is mounted on glass. Plus it is easier to repair LSIs than COG module.
We expect this development to be a method for developing new LCD module systems in the future.

Table 1 Specification of source driver LSIs.

Panel Driving Method	Line Inversion
Logic Voltage	2.7~3.6V
LCD Driving Voltage	3.0~5.5V
Clock Frequency	Max. 80MHz
Data Inputs	6bit×RGB
Simultaneous number of the coloring	64 gray scale 262,144 colors

Table 2 Specification of gate driver LSIs.

Logic Voltage	2.7~3.6V
LCD Driving Voltage	16.0~33.0V
Outputs Number	194/202 (Selectable)
Clock Frequency	Max. 250kHz

Acknowledgment

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