Ultra Low Power Consumption and High Definition: A 400dpi Reflective Storage Ferroelectric Liquid Crystal Display

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Abstract

Mobile products require longer battery lifetimes and increased information content from the display. A ferroelectric liquid crystal reflective storage mode is demonstrated. This display only needs updating when the image changes, giving ultra low power consumption. Passive matrix addressing allows for high resolution text to be displayed.

Introduction

The ever-increasing functionality of mobile information and communication tools means users will demand longer battery lifetimes and increased information content from the display interface of these products. Introducing a reflective display has significantly reduced the power consumption of portable devices (the backlight can consume more than 80% of the display power). However, current STN and TFT reflective display technologies still consume an unacceptable amount of power even when the display image remains fixed. This is because the liquid crystal mode must be continually refreshed in order to hold the image.
Typical books and periodicals are printed with resolutions from 600-1200dpi while typical printers achieve >300dpi. Currently LCDs rarely achieve greater than 200dpi because increasing the resolution of these displays either runs into fundamental addressing limits (STN) or increased cost (TFT). This means that the readability of text on displays is significantly poorer than that achieved on printed paper.

1. Advantages of Bistability

Surface stabilized ferroelectric liquid crystals (FLC)[1)] are intrinsically bistable and therefore do not need any power to display a fixed image. This bistability allows for an unlimited number of pixels to be addressed in a passive matrix. Both of these features make the FLC mode an ideal candidate for high resolution and low power displays.
Ferroelectric liquid crystals which exhibit a minimum response in the pulse width as a function of switching voltage have been developed due to improved multiplexibility, fast switching and high contrast[2)]. By lowering the spontaneous polarization, the voltage at which the minimum response time occurs also reduces, although the cost of this is a slower response time (**Fig. 1**). In a low power storage device the constraint on switching time is relaxed and it is more important to lower switching voltages for portable devices. For example a UXGA display updated at 5 pages/second would require a minimum line address time (l.a.t.) of 167µs (as opposed to the 12µs l.a.t. required for a video

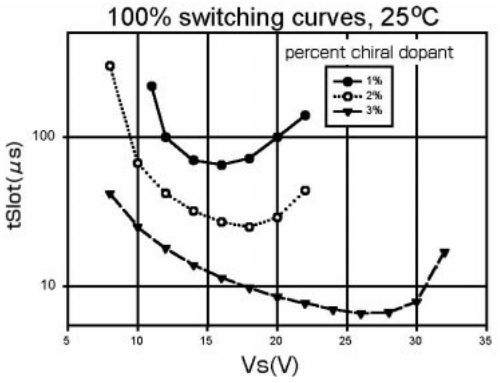

Fig.1 Effect of varying the chiral dopant on switching thresholds.

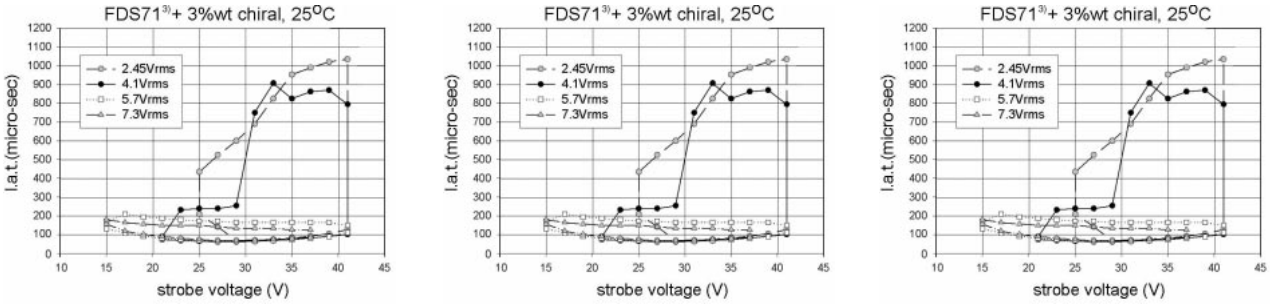

Fig.2 Drive windows for four different data voltages showing the effect of chiral dopant concentration (a) 3% (b) 2% (c) 1%.

rate HDTV FLC display[3]).

The operating range was determined using the DRAMA addressing scheme[4] which is designed to take advantage of the τ-Vmin response of these materials. A blanking pulse is applied with 6 slots of -Vs/2 followed by 2 slots of +Vs; this is then followed by a 0V period of 13 slots before the selection period. The selection period is 3 slots and consists of a 0V slot followed by 2 slots of +Vs; this is then followed by 1 slot of -Vs. The data pulse is {-Vd, +Vd, 0V} for a non-select (i.e. black) pixel and {+Vd,-Vd,0V} for a select pixel. In **Fig. 2a** the drive windows are shown for four different data RMS values with a 3% wt chiral dopant mixture. Note that fast line address times (<70μs) can be achieved using this material and addressing scheme however the operating voltages are large (>25V) when low data voltages are used. **Fig. 2b&c** show the drive windows for a 2% and 1% mixture respectively. Note that while the 1% mixture can operate at fairly low voltage, the line address times are too slow. The 2% wt chiral dopant mixture gave the best drive windows at low voltage. With this mixture it is possible to drive with strobe voltages as low as 15V and data voltages less than 3V.

2. Optical Configuration

In order to achieve a high contrast and high resolution reflective display we have optimized the FLC device for a single polarizer configuration. By using a single polarizer the reflector can be inside the device thus eliminating parallax. One obvious configuration is to make the FLC layer a quarter wave plate arranged to switch between 0° and 45° for white and black respectively. However this results in a black state which is highly chromatic resulting in a low contrast ratio. The chromaticity can be compensated with an external half-wave retarder[5] however the quarter wave plate condition for an FLC device results in a thin cell gap which is typically less than 1mm. It is also difficult to make a material with a 45° switching angle at 0V.

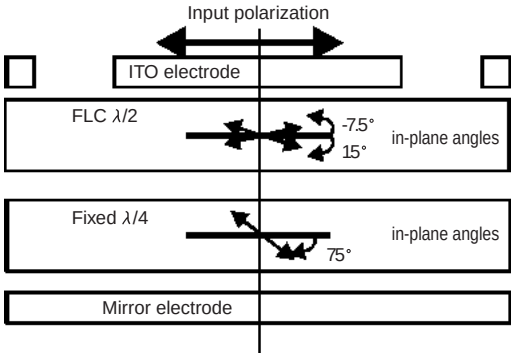

Fig.3 A single polarizer achromatic reflective configuration incorporatingan FLC half wave plate with a switching angle of 22.5° and a fixed quarter wave plate.

These problems are overcome by introducing a fixed quarter waveplate within the device. The combination of this quarter wave plate and the FLC layer are optimized to give achromatic black and white states by compensating the wavelength dependent retardation properties of the FLC layer (**Fig. 3&4**)[6]. Additional advantages are that the FLC layer can be the more reasonable thickness

of a half-wave plate (1.6μm) while the switching angle needs to be only 22.5°, a much more reasonable materials target.

A practical internal retarder is fabricated using reactive mesogen (RM) layers which can be spun down onto alignment layers and cured with UV light. These layers are robust and allow further device processing to be performed on top.

In order to achieve maximum contrast a material which gives a 22.5° switching angle at 0V is required. Much work has been done on ferroelectric materials which have up to 45° switching angles. However, due to the smectic layers forming a chevron structure, the zero volt effective memory angle (MA) is much less than 45° due to a triangular rather than uniform director profile (**Fig. 5**)[7]. When using the low pretilt C2 structure, the liquid crystal doesn't switch at the surface and the average memory angle reduces to around 18°. For high pretilt C1 structures, the liquid crystal does switch at the surface which increases this value to around 37°. Unfortunately neither low or high pretilt gives the correct memory angle.

To achieve 22.5° we would either need a material with a larger cone angle and aligned in the C2 mode or a material with a smaller cone angle and aligned in the C1 mode. Ideally we would also like this material to have a constant cone angle as a function of temperature. While most ferroelectric materials exhibit a second order phase transition giving a large temperature dependence of the cone angle, first order materials do exist and give almost constant cone angle throughout the SmC phase[8].

The temperature dependence of the second order material used here is shown in Fig. 6. This is the effective cone angle at 0V however it is possible to vary the effective cone angle by applying an AC voltage which couples to the dielectric biaxiality of the material (**Fig. 7**)[9]. This could in turn be used to compensate the change in cone angle as a function of temperature by applying a constant data voltage to the panel and varying the amplitude as temperature changes. Unfortunately, this type of compensation consumes power and therefore should be avoided. Further materials work in this area will therefore be needed to produce a temperature independent cone angle.

The device was optimized to give maximum contrast for a material with an 18° memory angle at 25°. By aligning the RM layer at 69° and the polarizer at –6°, relative to the rubbing direction, the optimal black state can be achieved at

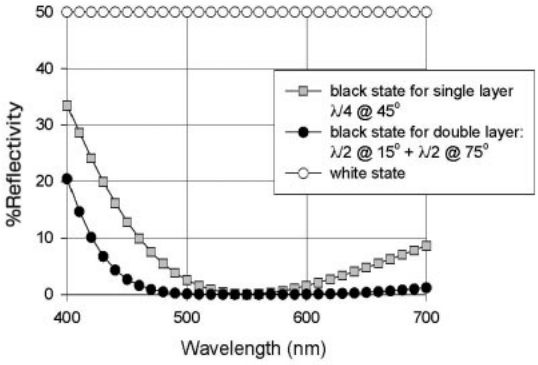

Fig 4 Achromatic optical performance of double layer device versus single layer device.

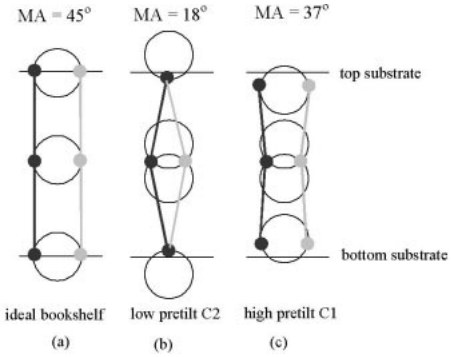

Fig.5 View of the director profile across the FLC layer for various alignment configurations (a) bookshelf (b) low pretilt a C2 chevron (c) high pretilt a C1 chevron.

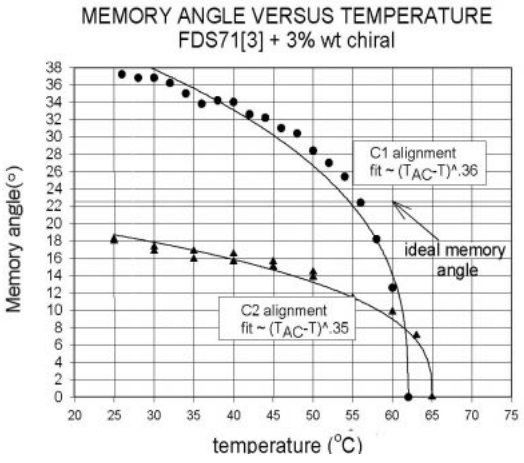

Fig. 6 Temperature dependence of the memory angle in C1 and C2 alignment.

the cost of reduced brightness. The theoretical reduction is shown in **Fig. 8**. Contrast ratios up to 45 have been measured at room temperature at normal incidence by subtracting the reflection from the top glass. More typical values using an external scattering film to produce off specular reflection are around 7. Ideally, an internal gain scatterer would be used as in the Sharp HR-TFT[10], although this bumpy surface has implications for the smectic alignment and optical performance of the device. The roughness of the surface could be planarized and under these conditions good smectic alignment would be obtained giving a brightness and contrast equivalent to that achieved in the HR-TFT.

3. Mechanical Stability

It is well known that the alignment quality of ferroelectric liquid crystals deteriorates when subject to mechanical shock. This is due to a disruption of the smectic layer structure which is unable to realign as easily as nematic alignment. Two types of mechanical damage mechanisms have been identified. Flow of the liquid crystal material occurs most easily within the smectic layers. However, if a barrier exists in the device (e.g. particulate, spacers, etc.), the material must permeate between layers. This destabilizes the C2 alignment structure and can induce a C2 to C1 flip in the chevron layer structure[11]. Shear between the display substrates can also destabilize the layer structure and induce a permanent damage texture[12].

Constructing polymer walls which extend perpendicular to the smectic layers and span the thickness of the device can reduce both flow and shear. This technique was shown previously to give mechanical stability thresholds of 200N/cm^2 which is similar to STN values[13] . In our device a lower density of polymer walls were used giving slightly lower thresholds for mechanical stability as shown in **Fig. 9**. Note the vast improvement over cells constructed with spacer beads. The width and type of wall material used have no effect indicating they are all equally inhibiting flow parallel to the smectic layers.

4. Reflective FLC Storage Demonstrator

To demonstrate the feasibility of high resolution FLC storage, a 300x300 matrix device at 400dpi resolution was fabricated (**Fig. 10&11**). The reflector is made of Al which

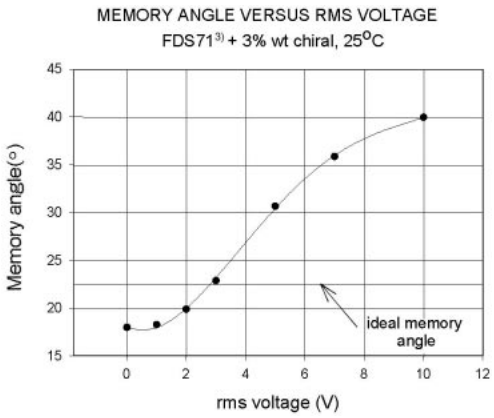

Fig.7 The dielectric biaxiality of the material couples to high frequency data voltages allowing for compensation of changes in memory angle.

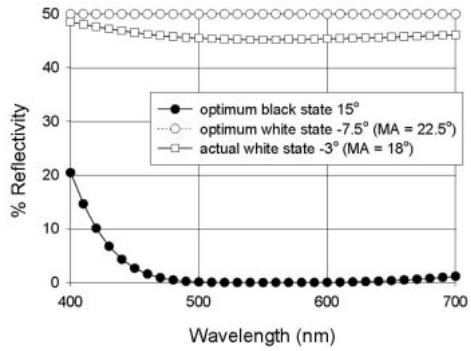

Fig.8 Contrast ratio is maximized by aligning the FLC layer such that the optimum black state is achieved. This results in a reduction in brightness due to the non-ideal 18° memory angle.

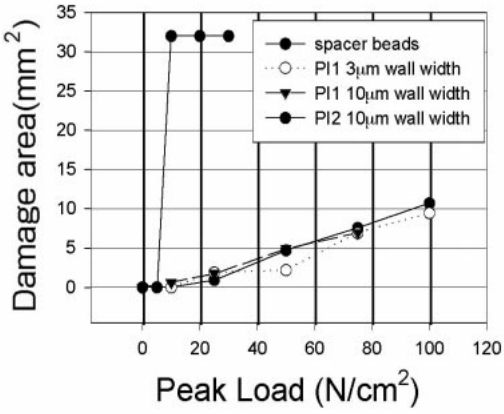

Fig.9 Mechanical stability of wall cells versus spacer cells.

is etched with 3µm gaps to act as one set of electrodes. An alignment layer is spun and rubbed to align a reactive mesogen which is spun and cured to give a quarter wave plate (0.8µm). A further alignment layer is spun and rubbed on top of the RM layer to align the FLC layer. On the counter substrate ITO is etched and polymer walls with a width of 3µm and height of 1.6µm are patterned in the interpixel gaps at a pitch of every 10 pixels. An alignment layer is spun and rubbed on top of these walls. The cells are then assembled and filled with the FLC mixture FDS71[3].

The lack of intrinsic greyscale is overcome by using error diffusion (**Fig. 10**). There is a trade-off between resolution and greyscale and using error diffusion[14] can dramatically reduce the number of greylevels required. Gille et al have shown that 150dpi with 8 greylevels and 600dpi with 2 greylevels are both equivalent to 120dpi with 256 levels when multibit error diffusion is incorporated. While the image quality of low resolution greyscale may be equivalent to high resolution binary, the text readability will be superior in the high resolution device and is therefore preferable.

The device operates at row voltages as low as 15V and data voltages as low as 3V for a line address time of 100µs. By etching down to 3µm interpixel gaps the aperture ratio can be 91%. Due to the small interpixel gaps, the fringing field between pixels is large enough to switch the FLC layer. Once the field is removed, the interpixel gaps remain switched due to the bistability of the material. This in turn gives an increased aperture ratio of 95% (**Fig. 10**). If the device structure was modified such that the reflective surface was continuous (this would require ITO electrodes on the bottom surface) then theoretically 100% aperture ratio could be achieved.

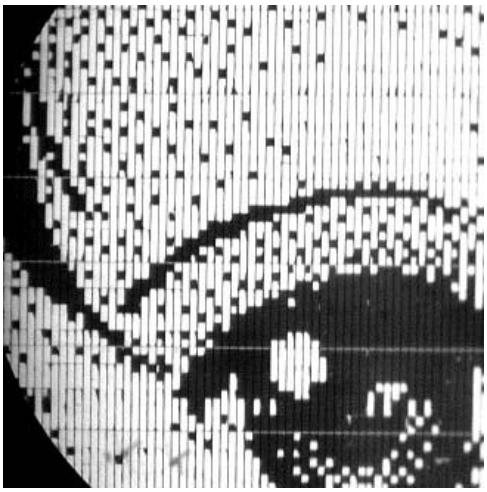

Fig.10 Greyscale is achieved using error diffusion. Interpixel switching gives 95% aperture ratio.

Conclusions

Reflective storage modes which only need updating when the image changes are a means of obtaining ultra low power consumption display devices. Passive matrix addressing of bistable modes allows for high resolution which improves image quality and text readability. By optimizing the FLC for a single polarizer reflective configuration it is possible to obtain a high contrast, parallax free, high resolution display. A 1" diagonal prototype was built showing images at 400dpi resolution with good contrast ratio, high aperture ratio and superb text readability (**Fig. 11**). Although intrisically black and white the display also showed greyscale images using

Fig. 11 Photographs of the 400dpi FLC displays after electrical connections have been cut showing that the images are stable with no power to the display.

error diffusion at high resolution. Good cell gap uniformity and mechanical stability were maintained with polymer wall spacing technology. We have demonstrated that the ferroelectric liquid crystal device is an ideal candidate for low power high resolution display applications.

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References

1) NA Clark and ST Lagerwall, "Sub microsecond bistable electrooptic switching in liquid crystals" Appl Phys Lett, (1980) 36, p899
2) PWH Surguy et. al., "The 'JOERS/Alvey' ferroelectric multiplexing scheme", Ferroelectrics, (1991) 122, p63
3) N Itoh et al, "17" video-rate full-color FLCD", IDW '98, p205
4) JC Jones and CV Brown, "The tVmin approach to ferroelectric liquid crystal displays", Euro Display '96, (1996) p151
5) GD Sharp, KM Johnson, US 5 658 490
6) MD Tillin, MJ Towler, K Saynor, S Gilmour, GB 2 318 878 and EP 0 840 160
7) MH Anderson et al, "Optical studies of thin layers of smectic-C materials" J Phys D: Appl Phys, (1991) 24, p338
8) M Isogai et al, Japan Display '86, (1986) p472
9) JC Jones, MJ Towler and JR Hughes, "Fast, high-contrast ferroelectric liquid crystal displays and the role of dielectric biaxiality", Displays, (1993) 14, p86
10) Y Ishii and M Hijikigawa, "Development of highly reflective color TFT-LCDs", Asia Display '98, (1998) p119
11) MJ Towler et al, "Permeative flow and the compatability of smectic C zig-zag defects with compresive and dilative regions" Liquid Crystals, (2000) 27, p75
12) N Wakita et al, "Shock-problem free FLCDs and mechanisms of alignment destruction by mechanical shock" Ferroelectrics, (1994) 149, p229
13) PA Gass et al, "FLCD mechanical stability, setting and achieving realistic targets", Proceedings of IDRC'97, (1997) pL-28
14) J Gille, R Martin and J Larimer, "Spatial resolution, grayscale, and error diffusion trade-offs: impact on display system design", Proc of IDRC '94 (1994) p381

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