Low-Temperature Stacked Gate Insulator by Photo Oxidation and PECVD for High-Performance TFT LCDs

Yukihiko Nakata[*1] Takashi Itoga[*2] Tetsuya Okamoto[*2] Toshimasa Hamada[*2] Yutaka Ishii[*3]

*1 Systems-LCD Group
*2 Engineering Development Dept. 1, Process Development Center, Systems-LCD Group
*3 Display Development Center, Display Technology Development Group

Abstract

A novel gate insulator formation method for Poly-Si TFTs was developed to reduce the process temperature and to improve the device performance. Excellent SiO_2/Si interfaces with an interface state density of 2-3x10^{10}/cm^2/eV was obtained by photo oxidation under irradiation of Xe excimer light at 200-300°C. This interface state density is the same as that of thermal oxidation at 950°C and is about 1/4 of the current standard gate insulator for Poly-Si TFTs. Also, a stacked film of a 3 nm photo oxide and a 40 nm PECVD film using TEOS gas without annealing has the same electric characteristics of the current standard gate insulator, in spite of the low process temperature and the film thickness being less than half of the standard one. The stacked gate insulator composed by photo oxide and PECVD film is promising in reducing process temperature and improving performance.

Introduction

With advances in information technology (IT), mobile displays have taken great strides toward becoming more compact with higher performance by consolidating numerous new functions in the display panel itself. Low-temperature poly-crystalline Si thin-film transistors (poly-Si TFTs) offer better electrical characteristics than conventional amorphous Si thin-film transistors (a-Si TFTs), and because they enable a variety of circuit logic to be formed directly on the glass display panel itself, hold out especially high promise. Continuous Grain Silicon (CG-Silicon), a type of poly-Si material, has higher electron mobility, and has properties that will bring higher performance to display panels.

One key technology of these low-temperature poly-Si TFTs is the formation of gate insulators. At present, an SiO_2 film formed by PECVD (plasma enhanced chemical vapor deposition) using TEOS (tetraethyl orthosilicate) gas is commonly used as the gate insulator in low-temperature poly-Si TFT. However, there are problems in applying this method to next-generation poly-Si TFTs. The first problem is that improvements in interface characteristics will be required to reduce the deviation in threshold voltage levels. Second, annealing at approximately 600°C for around 2 hours is required to improve the characteristics after film deposition. Third, it is difficult to obtain thinner films to enhance performance. And fourth, the carbon impurity concentration increases by an order of magnitude when the deposition temperature is reduced from the current 300°C to 200°C.

On the other hand, an oxidation process is useful to form the gate insulator with a good SiO_2/Si interface, because the interface is formed inside the Si film. Nevertheless, thermal oxidation typically employed in semiconductor processes cannot be used because the oxidation rate at temperatures below 600°C is too slow. For this reason, research is being conducted on a variety of low-temperature oxidation processes.

Fuyuki et al. carried out oxidation using active oxygen atoms produced by remote plasma[1]. And Ueno et al. were able to efficiently produce active oxygen radicals using a Kr/O_2 gas mixture, and indicated they were able to accelerate the oxidation rate[2]. Ohmi et al. proposed a method using a Kr/O_2 gas mixture and a new plasma source[3]. This method offers excellent interface characteristics regardless of the crystal orientation and is ideal for poly-Si TFTs. In addition, photo-oxidation also underwent a fundamental review[4].

These low-temperature oxidation methods were studied with the objective of applying them to integrated circuits with a film thickness of less than 5 nm.

However, these insulators around 5 nm in thickness used for integrated circuits cannot be applied to the poly-Si TFTs. This is because the insulator must be formed on a glass substrate having a surface area nine times larger than a silicon wafer, on top of poly-Si which has a high surface roughness while keeping the electrical defect density to a level below one in several hundredths. As a result, the current film thickness is approximately 80 to 100 nm.

Consequently, the objective of the present R&D is to develop low-temperature gate insulators with good SiO_2/Si interface for next-generation poly-Si TFTs. The gate insulator can eliminate high-temperature annealing after film forming and it is capable of reducing the film thickness to less than half of current levels.

1. Proposed approaches

Fig. 1 below shows the approach of using stacked films to achieve the aforementioned objective.

To lower the oxidation temperature, photo-oxidation was used because, unlike plasma-based oxidation, it has the outstanding feature of causing no plasma damage.

1) For the first layer, photo-oxidation is used to form a high-quality SiO_2/Si interface with good coverage.
2) For the second layer, a high-quality gate insulator, which has a leakage current and breakdown voltage equivalent to current gate insulators, is formed at low temperatures.

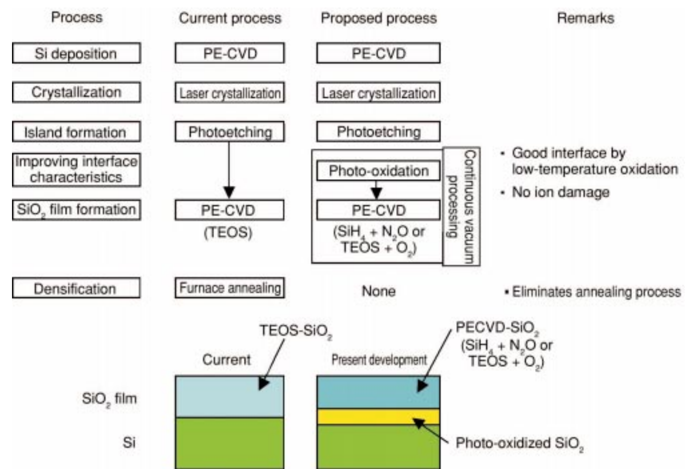

Fig. 1 Current and proposed process of gate insulator formation.

2. Photo-oxidation/PECVD equipment and experimental methods

The photo-oxidation/CVD equipment used in the present research is shown in **Fig. 2**. First, photo-oxidation of the substrate is carried out in a photo-oxidation chamber. Without breaking vacuum, the substrate is transferred to a CVD chamber, and an oxide film is continuously deposited by PECVD.

For photo-oxidation, the substrate is placed in the photo-oxidation chamber, the air evacuated, oxygen gas introduced, and pressure maintained at the desired level. After the substrate is heated by an IR lamp, the oxygen gas is irradiated by light at a wavelength of 172 nm from an Xe excimer lamp, disassociating the

oxygen gas and producing active oxygen radicals O (1D). When light of 172 nm is used, no ozone is created, and active oxygen radicals O (1D) can be generated efficiently by a single-process reaction. These active oxygen radicals O (1D) are more active than oxygen molecules and ozone and promote the oxidation reaction. In addition, a single-crystal Si wafer [p-type, (100), 8 to 12 ohm Ω cm] was used as a substrate to evaluate the SiO_2/Si interface. A bias temperature test (BT) was conducted under conditions of 150°C, ±2 MV/cm for 30 minutes.

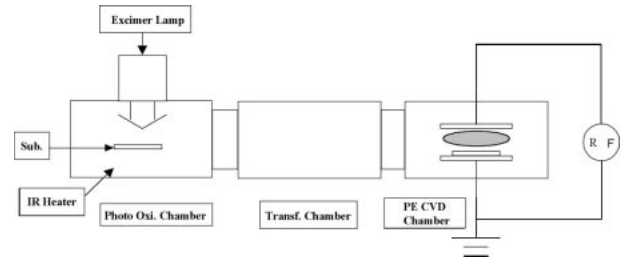

Fig. 2 Equipment for combination photo-oxidation and PECVD process

3. Oxide film thickness required to improve interface characteristics

Thermal oxidation was used to investigate how thick the first oxide film layer would need to be in order to improve interface characteristics in a stacked PECVD film. The thermal oxide film at 900°C can eliminate the effects of the oxide film quality. For the second layer, a SiO_2 film was formed by PECVD using SiH_4 + N_2O gas at an RF power of 100 W, making a total film thickness of 100 nm.

Fig. 3 shows the relationship between thermal oxide film thickness and interface trap density. For thermal oxidation films greater than 2 nm in thickness, the interface trap density was reduced to a value of a thick thermal oxidation film. Consequently, it was judged that interface characteristics can be significantly improved by forming a thin oxide film of around 2 nm.

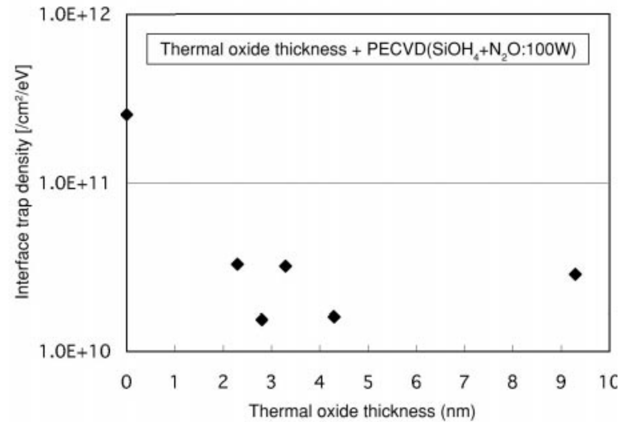

Fig. 3 Interface trap density vs. thermal oxide thickness at thermal oxide + PECVD stacked insulator.

4. Photo-oxidation

The photo-oxidation rate was measured under various conditions. The light of an Xe excimer lamp at a wavelength of 172 nm irradiates oxygen gases to generate active oxygen radicals and the oxygen radicals produce an SiO_2 film on the single-crystal Si wafer by oxidation.

Fig. 4 shows the relationship between photo irradiation time and the thickness of the photo oxide SiO_2 film. The substrate temperature was set at 300°C and the oxygen gas pressure was at 67 Pa. The light intensity measured at the substrate surface was 11 mW/cm^2. In the first oxidation stage, the

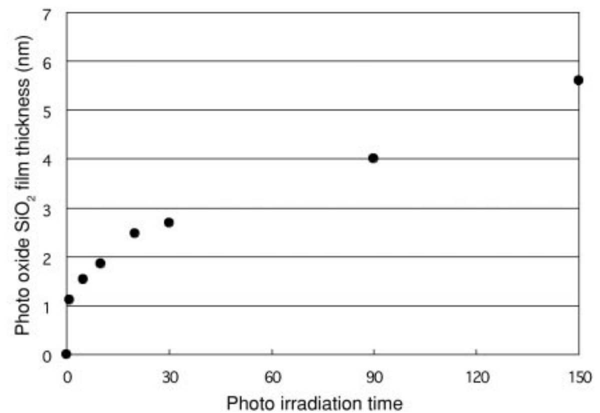

Fig. 4 Photo oxide SiO_2 thickness vs. photo irradiation time.

photo-oxidation rate is fast, and a 1.1 nm thick film was produced in one minute of photo irradiation, but thereafter it slowed, exhibiting a tendency toward saturation. Presently, an Xe excimer lamp with a power of 30 mW/cm^2 is commercially available, and improvements in the photo-oxidation rate are possible.

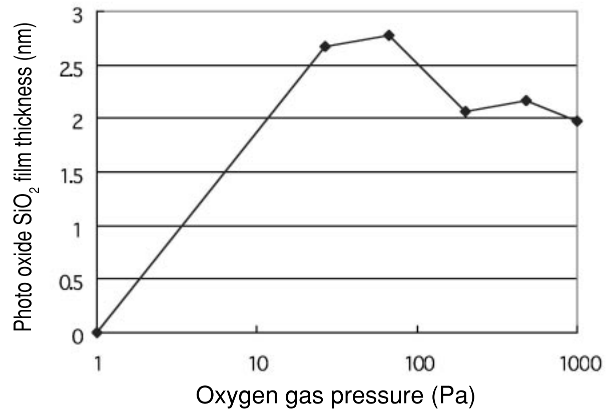

Fig. 5 Photo oxide SiO_2 thickness vs. oxygen pressure.

Fig. 5 shows the relationship between the oxygen gas pressure and the thickness of the photo oxide SiO_2 film. The substrate temperature was set at 300°C. A peak in the photo-oxidation rate exists between gas pressures of 20 to 70 Pa. At high oxygen gas pressure, light enters from the transmission window and is quickly absorbed near the window, and thus, the oxygen radicals are generated at a place far from the substrate. At low oxygen gas pressure, few active oxygen radicals are generated. In both cases, the photo-oxidation rate is reduced, and it would appear that an optimal oxygen gas pressure exists.

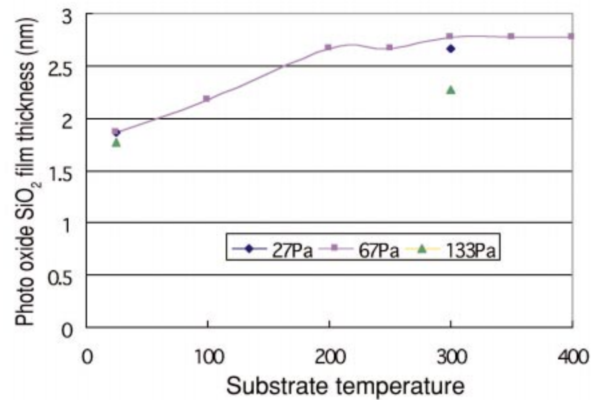

Fig. 6 Photo oxide SiO_2 thickness vs. substrate temperature.

Fig. 6 shows the relationship between the substrate temperature and the thickness of the photo oxide SiO_2 film after 30 minutes of photo-oxidation. As the substrate temperature increased from 25°C to 200°C, the photo-oxidation rate increased by about 1.5 times. In addition, the photo-oxidation rate was the same at substrate temperatures from 200°C to 400°C. And the results of FTIR (Fourier transform infrared ray) spectroscopy measurements of the wave number of the Si-O bond showed the same film quality from 200°C to 400°C, and an excellent film can be obtained even at low temperatures.

5. Photo oxide + PECVD (SiH_4+N_2O) stacked insulator properties

After using photo-oxidation to form a 3-nm SiO_2 layer, the second SiO_2 film was deposited by PECVD with SiH4 and N_2O gases. **Fig. 7** shows the interface trap density (Dit) of photo oxide and PECVD (SiH4+N_2O) stacked films. Using photo-oxidation to form the SiO_2/Si interface, an interface trap density of 2-3x10^{10}/cm^2/eV was obtained at 200°C. This is about the same as the typical value of 2-4x10^{10}/cm^2/eV obtained by thermal oxidation at 950°C, and is about one-fourth of that obtained by PECVD (SiH_4+N_2O) normally employed.

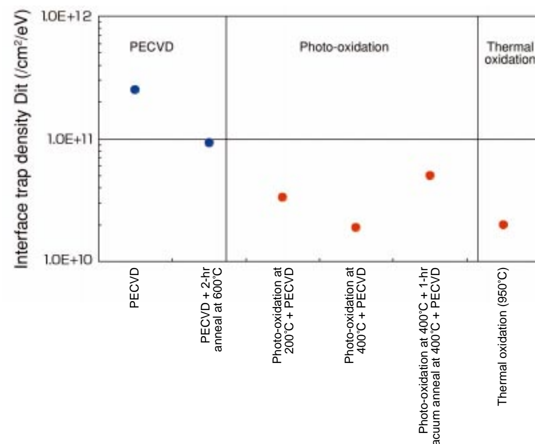

Fig. 7 Interface trap density of photo oxide + PECVD (SiH_4+N_2O) stacked insulator.

However, in the stacked insulator in which the second SiO_2 layer was formed by PECVD using SiH_4 and N_2O gases, the flat band voltage (Vfb) changed in a BT test. It is possible that this is the result of residual nitrogen in the SiO_2 film.

6. Properties of the photo oxide + PECVD (TEOS+O_2) stacked insulator

To improve the reliability, a stacked film that used an SiO_2 film formed by PECVD with TEOS + O_2 gases was evaluated. **Fig. 8** shows the relationship between film thickness and Vfb for a PECVD film (TEOS + O_2) formed on top of a 3-nm-thick photo oxide film. The thinner the PECVD (TEOS + O_2) film layer, the smaller the value of |Vfb| according to the ordinal rule. In a stacked insulator consisting of a 3-nm-thick photo oxide film and a 40-nm-thick PECVD (TEOS + O_2) film, the Vfb value was -1.4 V and the ΔVfb value of the -BT test was -0.5 V. These values are close to the Vfb value of -1.1 V and a ΔVfb value of the -BT test of -0.6 V measured for a PECVD (TEOS + O_2) film (film thickness: 100 nm) annealed at 600°C for 2 hours.

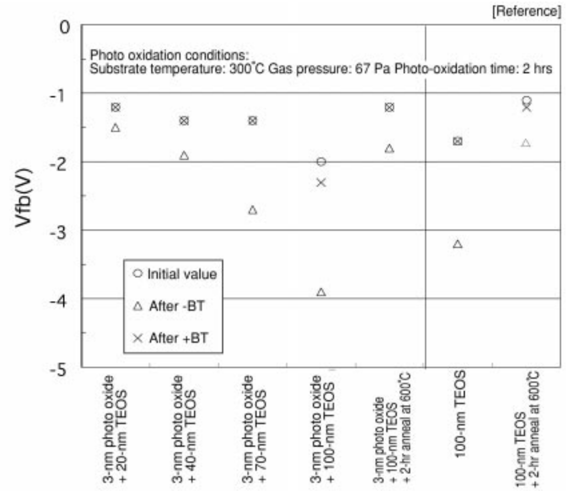

Fig. 8 Flat band voltage of photo oxide + PECVD (TEOS+O_2) stacked insulator.

Fig. 9 shows the interface trap densities of the same samples. With a stacked insulator consisting of a 3-nm-thick photo oxide film and a 20-nm-thick PECVD (TEOS + O_2) film, an interface state density of 2x1010/cm^2/eV was obtained. The thicker the PECVD (TEOS + O_2) film, the greater the interface trap density. The thicker the film, the longer the plasma exposure time during film formation, and this phenomenon is thought to be the result of deterioration of the SiO_2/Si interface caused by plasma damage.

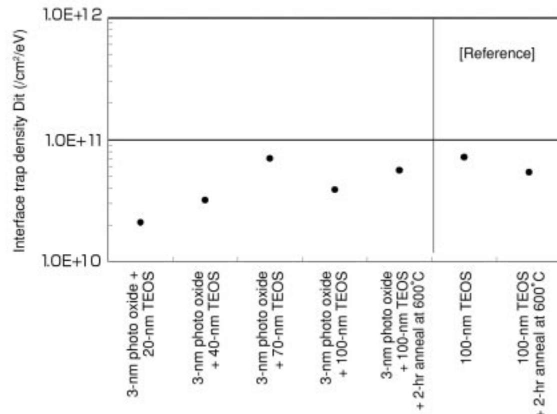

Fig. 9 Interface trap density of photo oxide + PECVD (TEOS+O_2) stacked insulator.

Fig. 10 shows the relationship of the current density (J) and electric field strength (E) in the same samples. A 3-nm-thick photo oxide + 40 nm PECVD (TEOS + O_2) stacked film has the leakage current (current density J when electric field strength E = 2 MV/cm) below $1x10^{-10}$ A/cm^2.

The breakdown voltage (electric field E when current density J = $1x10^{-6}$ A/cm^2) was greater than 8 MV/cm, regardless of the thickness of the PECVD (TEOS + O_2) film on top of the photo oxide film.

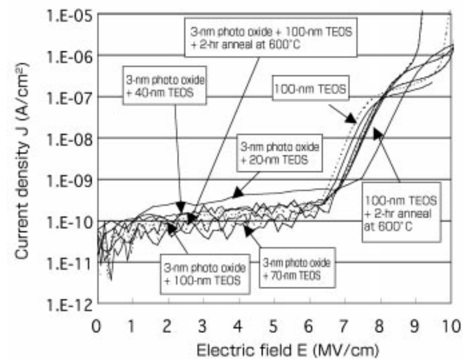

Fig. 10 Current density-Electric field charactenstics photo oxide + PECVD (TEOS+O_2) stacked insulator.

Conclusions

A method of forming gate insulators for poly-Si TFTs was developed to reduce the process temperatures and improve the interface characteristics.

An excellent SiO_2/Si interface with an interface trap density of 2-3x10^{10}/cm^2/eV was obtained by photo-oxidation under irradiation by an Xe excimer lamp at a substrate temperature of 200 to 300°C. This interface trap density is equivalent to that of thermal oxide at 950°C and is about one-fourth of the current standard gate insulators used in poly-Si TFTs.

In addition, a 3-nm photo oxide and 40-nm SiO_2 PECVD stacked film using TEOS gas has the same electrical characteristics as the standard poly-Si TFT gate insulators in spite of lower process temperatures and less than half the film thickness.

The stacked gate insulator derived from these photo oxide and PECVD films offers significant advantages in terms of lower process temperatures and improving the performance of poly-Si TFTs.

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References

1) T. Fuyuki, T. Oka and H. Matsunami, Jpn. J. Appl. Phys. Vol. 33, 440 (1994).
2) T. Ueno, A. Morioka, S. Chikamura and Y. Iwasaki, Jpn. J. Appl. Phys. Vol. L327 (2000).
3) M. Hirayama, K. Sekine, Y. Saito and T. Ohmi, IEDM Tech. Dig., 249 (1999).
4) J.Y. Zhang and I.W. Boyd, Appl. Phys. Lett. 71, 20, 2964 (1997).

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